International Journal of Contemporary Technology and Management
Volume VI, Issue VII, July - 2017 ISSN (Online) 2278-8034

Implementation of Static RAM with Sleep Transistor to Leakage Power Reduction

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ABSTRACT: In the paper we are working on the circuit level implementation of the SRAM cell. The SRAM cell has six transistors and therefore we call it 6T SRAM. A bulk 6T SRAM is implemented and simulates for the proper functioning of the SRAM cell for 1 bit storage. We are working on the 90nm technology. We are using DG-MOSFET for reducing the threshold voltage and so the power consumption. On the circuit level, the static power dissipation is come to account. This static power dissipation is caused by a major factor that is leakage current. The reduction of leakage current is done by using Sleep Transistor technique. The DG-MOSFET based 6T SRAM with Sleep Transistor technique is implemented and simulated. The designing and simulation tool we used is Cadence virtuoso. The transient, dc and parametric analysis provide the results. The transient response helps to show the proper function of SRAM and dc response provides the results related to the voltage values which are helpful to know about the power consumption of the circuit. The parametric analysis gives different values of leakage current on different width of the MOSFET which shows that the bulk 6T SRAM consumes more power than DG-MOSFET based 6T SRAM with Sleep Transistor.

1. INTRODUCTION

Recent memory technologies including SRAM, DRAM and flash memory are facing technology limits to their continued upgrading. Accumulation of new materials to improve gate SiO_2oxide concert and consistency can only add to circuit costs. This fact has led to intense efforts to ripen new memory technologies. This type of memory which addressed is primary and secondary memory which is volatile but BIOS battery helps to provide them power supply to be in hold mode. Most of these new technologies are less affected by short channel effect on memories and can be used for long term storage or to provide a memory that does not lose information automatically. DG-MOSFET based SRAM cells will begin a new substitute to CMOS based SRAM and DRAM cells in a next few years. The rate of development of compact memories more and more with fewer amounts of its drawbacks helps to replace CMOS technologies to DG-MOSFET based emerging technologies. Moving to a DG-MOSFET based disk and cache devices will reduce power usage and dissipation directly as well as with new

power saving modes, and it provides the better performance in lesser channel length. The use of a double gate technology as an embedded memory with CMOS logic has countless job the electronics industry.

2. IMPLEMENTATION AND DESIGN

6T SRAM Cell

As SRAM cell is the most traditional circuit in system on chip (SoC) technology which scales down size of cell and also voltage. 6T SRAM cell have total of six transistors in which four are NMOS and two are PMOS. Out of six, four transistors i.e. NMOS and PMOS transistors combines to form a pair of inverters in bi-stable latched format and the other two NMOS transistors (N3 & N4) are used to pass bit line data in bi-stable latched that shown in Figure 1.

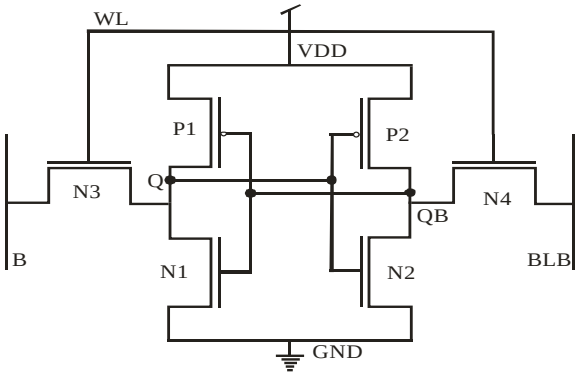


Figure 1 Conventional 6T SRAM Cell

In 6T SRAM Cell there are two bit lines BL and BLB which are complement of each other but of same period and Q and QB are also complemented outputs and a single word line WL. There are three modes of operation in SRAM cell i.e. Hold mode, active mode, stand-by mode. In stand-by mode WL goes high to low (WL=0) and the bit line either 0 or 1, it just holds the data inside the cross coupled inverters.

In write mode, word line goes low to high (WL=1) and new data is put into BL bit line, that data writes on Q and QB outputs using pass transistors. When word line goes high to low (WL=0) and the data on bit line (BL) is pre-charged or left floating, the value stored during write operation at output Q goes through pass transistor to one of bit line that is discharging and another one line is pre-charging and this charging and discharging of data is sense by sense amplifier during read operation and amplifies the data which is used further at outputs Q and QB.

PROPOSED DG-MOSFET BASED SRAM CELL

The memory design is very simple just to hold single bit data. The memory that we are using in our application purpose is the 1-bit of memory due to that data retention and power dissipation in are major issues, so future requires technology which has scaling capability itself to reduce size because of that DG--MOSFET becomes point of line for this issue. For better reduction in short channel effects, power supply scaling capability, low power dissipation, DG-MOSFET is superior choice than conventional CMOS.

The MuGFET based CMOS technology on SRAM cell and E-memory that helps to cell stability issues, reduced leakage current, and

better device mismatch. The low power design is suitable through DG-MOSFET due to no body biasing for leakage reduction and it works on less power supply voltage compare to CMOS logic.

DG-MOSFET width needed efforts to design SRAM cell by adjusting V_{th} of SRAM cell. So we design 6T SRAM cell using model and studied in different voltages.

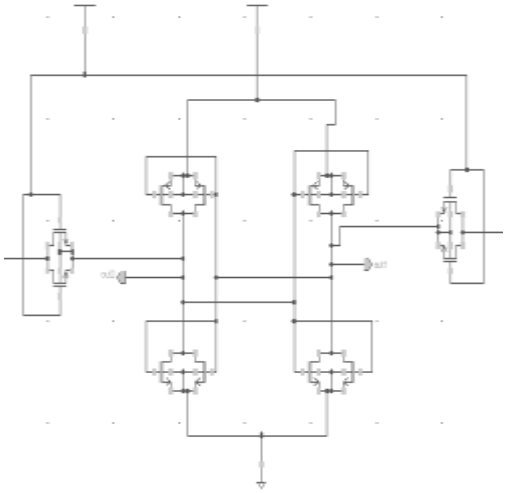


Figure 2 DG-MOSFET based 6T SRAM Cell

POWER CONSUMPTION

Power consumption is now the major technical problem facing the semiconductor industry. For a digital circuit, the overall power dissipation, includes two components these are: - dynamic power and static power dissipation.

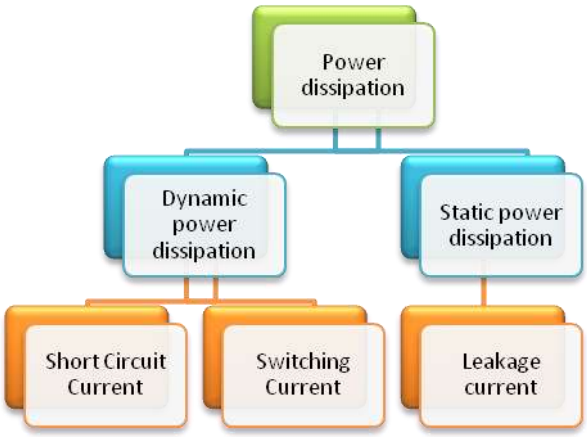


Figure 3 Hierarchy of the Power Dissipation

The hierarchy helps to understand the way by which the power dissipation gets affected by the currents. The dynamic power dissipation is occurs due to the short circuit and switching current whereas the static power dissipation occurs due to the leakage current. Total power dissipation is expressed as-

$$P_{total} = P_{dynamic} + P_{static} \quad (1)$$

Where $P_{dynamic}$ = dynamic power dissipation.

P_{static} = static power consumption

Dynamic power

Dynamic power dissipation is occurs due to the charging and discharging of the capacitor as well as the frequency.

The average dynamic power consumption is given by-

$$P_{dynamic} = C_L V_{DD}^{\ 2} f \quad (2)$$

Where,

$\mathbf{C_L}$ is the switching capacitance,

$\boldsymbol{f}$ is the operating frequency.

$\mathbf{V^2_{dd}}$ is the supply voltage

Short Circuit Power Dissipation

The short circuit power dissipation occurs due to the short circuit current that are occurs when the higher voltage in the system gets path directly to the ground is called the short circuit power dissipation. It is expressed as:

$$P_{sc} = I_{mean} V_{dd} \quad (3)$$

$$I_{mean} = \frac{1}{T}\int_0^T I(t)dt \quad (4)$$

Switching Power dissipation

The charging and discharging of capacitance occurs losses the power is known as switching power dissipation.

Static power

The static power consumption can be given as-

$$P_{static} = V_{DD} * I_{static} \quad (5)$$

Where, t_{avg} = Average gate delay, t_{dr} = Rise time delay and t_{df}= fall time

Leakage current

One of the most important characteristics of ideal CMOS technology is the fact that it doesn't exhibit any magnitude of static power dissipation in steady state. In practical situations though, degraded levels of voltage are fed to gate comprising of CMOS transistors and a subsequent flow of current can be seen from power supply to ground, which is often termed as static biasing current. In Fig. 4, depicts the situation in which an inverter is driven by a pass transistor. On analyzing the circuit, we reach to the result that voltage at node A is degraded (V_{dd}-V_{th}). The inverter input being high (V_{dd}-V_{th}), the output would be low. Since, the PMOS transistor is weakly ON which results in static biasing current from power supply to ground nodes. Thus static biasing current come into the picture due to the aforesaid conditions. Static currents which flow from V_{dd} to ground, without degrading the inputs is known as leakage power. With the advent of technology resulting in scaling, supply voltage must be reduced to address dynamic power and issues pertaining to reliability. This in turn needs scaling of the device threshold voltage (Vth) so that a reasonable gate over drive can be maintained. Reduction in Vth, results in the subthreshold current to increase exponentially.

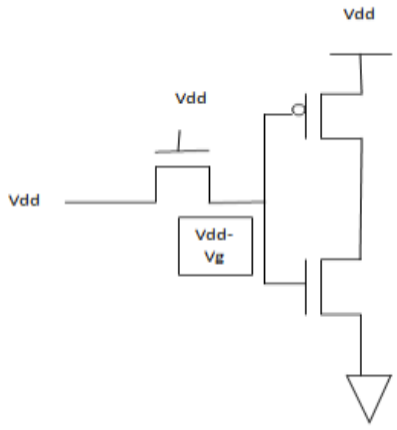


Figure 4 Degraded voltage level at the input node of a CMOS inverter results in static biasing power consumption

During the condition Vgs<Vth, the NMOS is off-state. Still, an unwanted value of leakage current might flow from the drain terminal to the source terminal. The current observed in the

MOSFET at Vgs<Vth is called the subthreshold current. This subsequently results in MOSFET off-state current, Ioff. Ioff is the Id measured at Vgs=0 and Vds=Vdd. It becomes mandatory for Ioff to have a very small value so that the circuit consumes negligible static power (typically in stand by mode)

As an illustration, let us consider Ioff be 100nA per transistor, a simple cell-phone chip that contains 100,000,000 transistors would consume almost a standby current (10A) that would result in the battery draining out briskly even without the cell phone getting any call. A desk-top computer may still be used but at the cost consuming power from the a.c. mains supply or UPS and moreover causing excessive heating problems. When Vgs is below Vth, Ids behaves as an exponential function of Vgs.

Fig. 5 depicts the subthreshold current. When Vgs is below Vth, the concentration of inversion electron (ns) is quite small but still it can result in a small leakage current to flow between the source and the drain terminals. In Fig. 5 (a), a large value of Vgs would pull Ec at the surface closer to Ef, causing ns and Ids to increase. From the equivalent circuit in Fig. 5 (b), it can be observed that:

$$\frac{d\varphi_s}{dV_{gs}} = \frac{C_{oxe}}{C_{oxe}+C_{dep}} \equiv \frac{1}{\eta} \qquad (6)\ \eta = 1 + \frac{C_{dep}}{C_{oxe}}$$

(7)

Integrating Eq. (6) yields

□ □φ_s□ □ □$constant + \frac{V_g}{\eta}$

□ □□(8)

Ids is proportional to ns, therefore

$I_{ds} \propto$□$n_s \propto e^{\frac{\varphi_s}{kT}} \propto e^{q(constant+\frac{V_g}{\eta})} \propto e^{\frac{qV_g}{\eta kT}}$

(9)

The practical definition of Vth in experimental studies is the Vgs at which Ids=100nA ×W/L. (Some companies may use 200nA instead of 100nA.)**1**. Eq. (9) may be rewritten

$$I_{ds}(\text{nA}) = 100 \,.\, \frac{W}{L} \,.\, e^{\frac{q(V_{gs}-V_{th})}{\eta kT}} \qquad (10)$$

Clearly, Eq. (10) agrees with the definition of Vth and Eq. (9). Considering the fact that the fuction exp(qVgs/kT) changes by 10 for every 60 mV change in Vgs, hence exp(qVgs/ hkT) changes by 10 for every h×60mV. As an illustration, if h=1.5, Eq. (10) states that Ids drops by 10 times for every 90mV of decrease in Vgs below Vt. h×60mV is called the subthreshold swing and represented by the symbol, S.

$$S = \eta \,.\, 60 \text{ mV} \,.\, \frac{T}{300} \qquad (11)$$

$$I_{ds}(\text{nA}) = 100 \,.\, \frac{W}{L} \,.\, e^{\frac{q(V_{gs}-V_{th})}{\eta kT}} = 100 \,.\, \frac{W}{L} \,.\, 10^{\frac{q(V_{gs}-V_{th})}{S}} \qquad (12)$$

$$I_{off}(\text{nA}) = 100 \,.\, \frac{W}{L} \,.\, e^{\frac{-q(V_{th})}{\eta kT}} = 100 \,.\, \frac{W}{L} \,.\, 10^{\frac{-V_{th}}{S}}$$

(13)

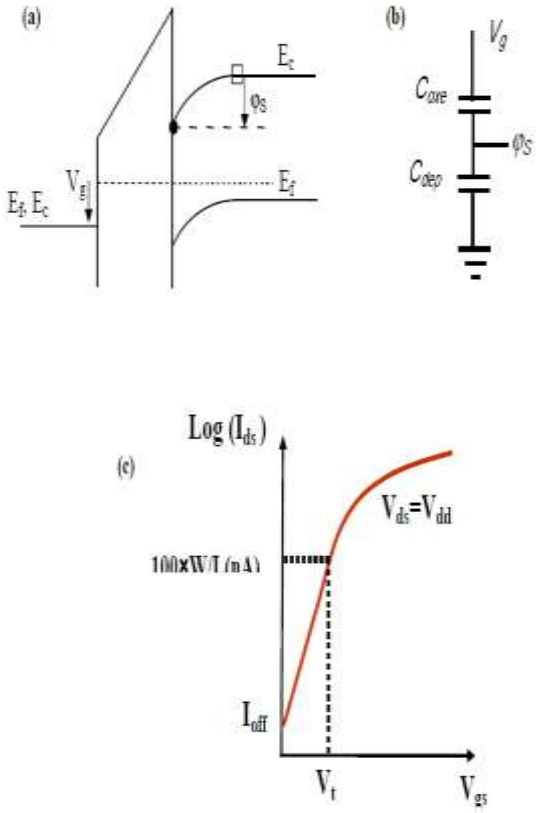


Figure 5: (a) When Vg is increased, Ec at the surface is pulled closer to Ef, causing ns and Ids to rise; (b) equivalent capacitance network; (c) Subthreshold IV with Vt and Ioff

There are two ways to minimize Ioff illustrated for some given value of W and L shown in Fig. 5 (c). One is choosing a large value of Vth, but this is not an optimal solution since it would reduce Ion and hence increase the gate delays. The other more feasible solution is to reduce the subthreshold swingn (S). S can be reduced by reducing h. That can be done by increasing Coxe (see Eq. 7), i.e. using a thinner Tox, and by decreasing Cdep, i.e. increasing Wdep. Another way to reduce S is to reduce Ioff, so that the transistors operate at a lower temperature. The last mentioned technique is seldom used for the additional cost that cooling needs.

Leakage reduction

The effect of self heating can be attributed to the presence of parasitic effects which affect circuits even at room temperature ($27^{\circ}C$). In CMOS circuits, the active mode of operation sees the effect of both static and dynamic power dissipation contributing to the overall power dissipation. In standby conditions, the main contributor to power dissipation is leakage current. As discussed earlier, as the scalability of the devices increase to incorporate more and more transistors on a chip, the leakage power grows substantially thereby limiting or even hindering the operation and application of the device**.**

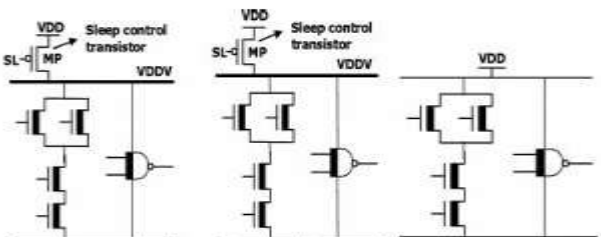
Thus to enhance the applicability of circuits under limited and low power conditions, leakage power dissipation has to be reduced. This can be done at both circuit and process or fabrication levels. Leakage at the process level can be reduced by controlling the dimensions (length, oxide thickness, junction depth, etc.) and manipulating the doping profile in transistor. At circuit level, Power gating techniques can be utilized by exploring supply and threshold voltage leakage dependence.

Power gating technique reduces leakage current primarily by reducing the power supply voltage. It uses a MOSFET switch (sleep transistor) to

cut off, or gate, a circuit from the power rails (Vdd and/or gnd) during conditions of standby. The power gating switch is generally connected between the power supply and the circuit and the circuit and the ground. These are the two interfaces of connecting the sleep transistor switch. During active mode of operation, the power gating switch is kept on, thereby supplying current to the circuit. During conditions of standby, the sleep transistor cuts off the circuit from the power supply thereby reducing the power.

The sleep transistor reduces leakage current due to two reasons. Firstly, the width of the sleep transistor is usually kept lesser than the total width of transistors being gated. A smaller width provides a linear reduction in the total current drawn from supply node during standby mode.

Secondly, leakage current values plummet whenever stacks of transistors are turned off due to the source biasing effect. Degradation in circuit performance is observed in due to the same effect in active mode. Although the on-resistance of the power gating switch is much lesser in magnitude compared to magnitude of off-resistance, still it creates a small positive voltage at the virtual node. Also, these voltages reduce the drive capability and bring about an increase in the threshold voltage of the NMOS devices by virtue of body biasing.



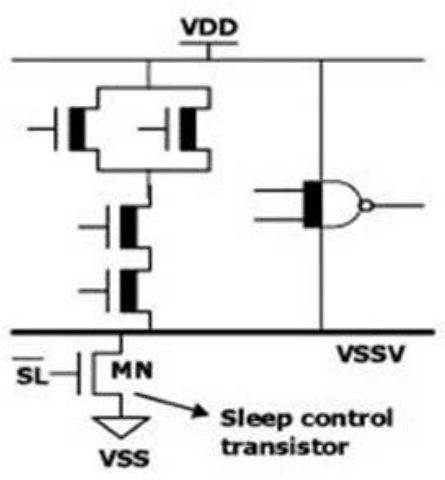


Figure 6 Schematic of Sleep Transistor circuit

Threshold Voltage

We are using DG-MOSFET for the implementation of SRAM cell which reduce the threshold voltage of the SRAM circuit. For the bulk SRAM, there are 6 transistor works on a minimum voltage or threshold voltage of 0.7V. In the implementation of SRAM with the help of DG-MOSFET uses two transistors which reduce the threshold by 2 as 0.35V. The supply voltage and Sink voltage are same as bulk SRAM but the number of transistors increases by using DG-MOSFET. Hence the length of the channel reduced and the threshold. It is a bid advantage of using DG-MOSFET as the data can be captured within a lower voltage limits which helps to reduce the power consumption of the circuit.

Supply Voltage

As we know about the threshold voltage reduction in the previous section, threshold reduction provides lesser supply voltage

requirement. If the bulk SRAM works on 5V V_{dc} , then the DG-MOSFET based SRAM works on just half of that voltage as 2.5V or we may take it as 3V. There is no need to apply more than 3V for the circuit.

Data Retention Voltage

Data retention voltage can be defined as the lowest possible power supply voltage at which the data can be retained inside the SRAM. Supply voltage takes down to achieve Data Retention Voltage (V_{dr}) to retain data in standby mode. DG-MOSFET based SRAM cell Data Retention voltage has lesser value than conventional based SRAM cell.

We have implemented a DG-MOSFET based 6T SRAM which uses the Sleep Transistor technique of leakage reduction. In our circuit the four parameters reduces as leakage current by using Sleep Transistor technique, Threshold, supply and data retention voltage by using DG-MOSFET. Hence the circuit consumes less power compared to bulk SRAM and dissipate less power.

3. SIMULATION AND RESULTS

we represent the simulation waveform of the three types of analysis:

1. Transient Analysis of the input and output circuits.
2. DC Analysis of the DC voltage source.
3. Leakage current Analysis

All the above analysis are done for four types of circuit, first is the 6T SRAM, second is the DG-MOSFET based 6T SRAM, third is 6T SRAM with Sleep Transistor and DG-MOSFET based 6T SRAM with Sleep Transistor.

We also compare the bulk 6T SRAM and DG-MOSFET based 6T SRAM with and without Sleep Transistor by the variation of the feature size. We are working on the 90nm technology so that the length of the MOSFET is considered as 100nm, the width can be varied and we are taking different width for the different feature size. The leakage current can be calculated for the different feature size and comparison is done between the bulk SRAM and DG-MOSFET based 6T SRAM with and without Sleep Transistor.

By doing all the above analysis and comparison we can easily find the precise applicability of the circuit in different VLSI systems. The analysis and comparison provides the better performance of DG-MOSFET based 6T SRAM over Bulk SRAM with Sleep Transistor technique so that we prefer DG-MOSFET based 6T SRAM with Sleep Transistor technique for getting low power dissipation.

Figure 7 shows the circuit of the bulk 6T SRAM cell and Figure 8 shows the proposed DG-MOSFET based 6T SRAM cell. Figure 9 shows the transient response of the bulk 6T SRAM cell and Figure 10 shows response of the proposed DG-MOSFET based 6T SRAM cell by cadence virtuoso tool using the process technology at 90nm, with the minimum supply voltage 0.7V.

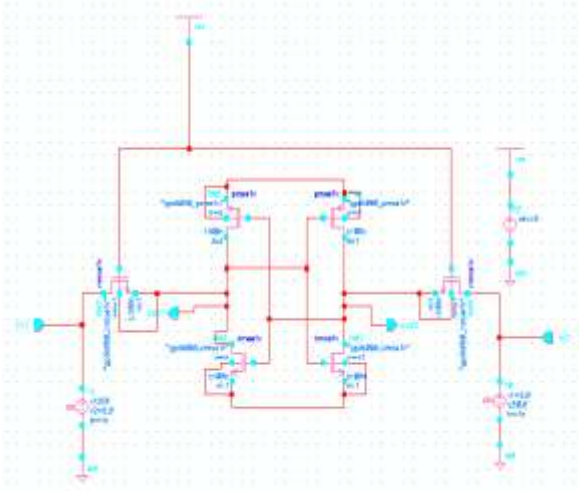


Figure 7 Circuit of the bulk SRAM Cell

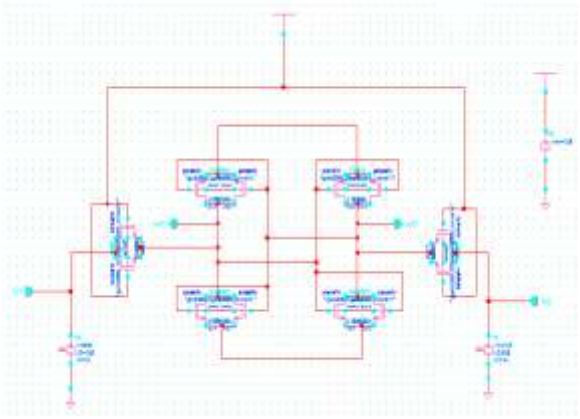


Figure 8 Circuit of the DG-MOSFET Based 6T SRAM Cell

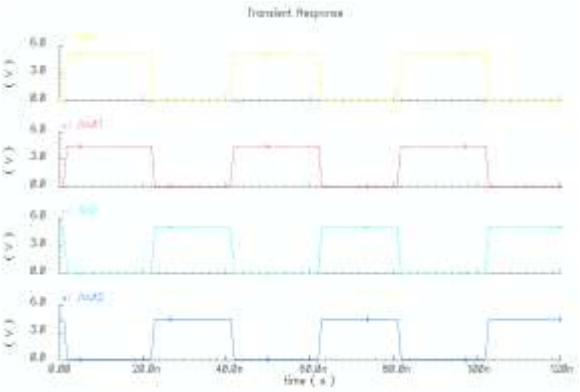


Figure 9 Transient Response of the bulk SRAM Cell

The above simulation result shows that the bulk 6T SRAM works well as it stores 1 bit of data according to the input pulse range. In the diagram four waveforms are shown. First waveform is the input to the SRAM of the range 0 to 5V for 120ns. The second waveform is the output of the first waveform which is same as input and provide accurate information to the output. The third waveform is the second input to the SRAM of the range 5 to 0V for 120ns. The fourth waveform is the output of the first waveform which is same as second input but invert of the first input which is required according to the functionality of the SRAM.

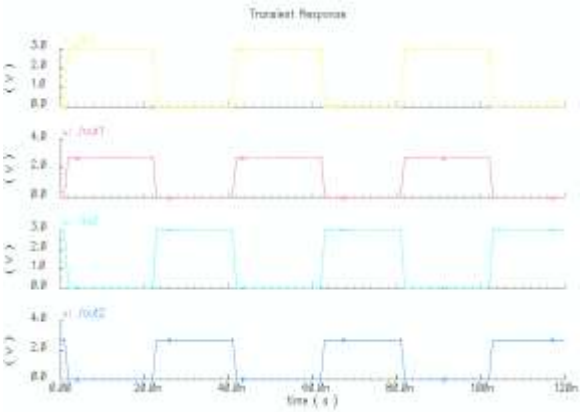


Figure 10 Transient Response of the Proposed DG-MOSFET Based 6T SRAM Cell

The above simulation result shows that the DG-MOSFET based 6T SRAM works well as it stores 1 bit of data according to the input pulse range. In the diagram four waveforms are shown. First waveform is the input to the DG-MOSFET based 6T SRAM of the range 0 to 3V for 120ns. The second waveform is the output of

the first waveform which is same as input and provide accurate information to the output. The third waveform is the second input to the DG-MOSFET based 6T SRAM of the range 3 to 0V for 120ns. The fourth waveform is the output of the first waveform which is same as second input but invert of the first input which is required according to the functionality of the SRAM.

From the above two circuits it is clear that the circuits work well and the function of the SRAM are perfect in both of them.

Figure 11 shows the transient response of the bulk 6T SRAM cell and Figure 12 shows response of the proposed DG-MOSFET based 6T SRAM cell.

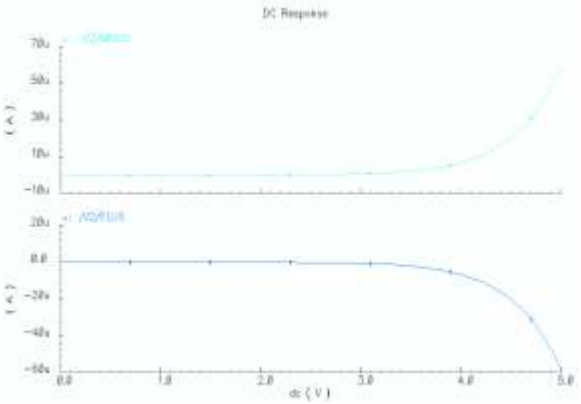


Figure 11 DC Response of the bulk SRAM Cell

From the above figure it is seen that the applied dc voltage to the circuit is 5V. The two waveforms are shown in which first one is the values getting from the negative terminal of the dc voltage source and the second one is from the positive terminal of the dc voltage source.

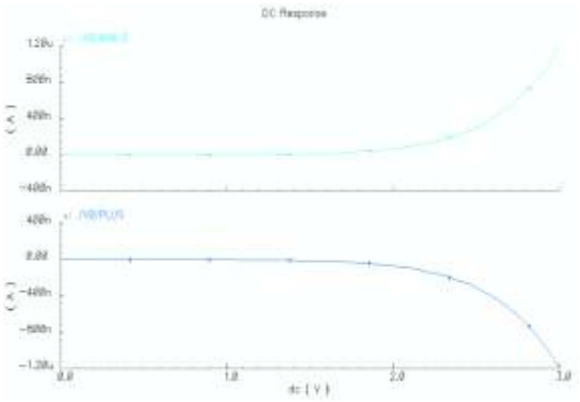


Figure 12 DC Response of the Proposed DG-MOSFET Based 6T SRAM Cell

From the above figure it is seen that the applied dc voltage to the circuit is 3V. The two waveforms are shown in which first one is the values getting from the negative terminal of the dc voltage source and the second one is from the positive terminal of the dc voltage source.

Now the leakage current is being calculated. As we know that the leakage current is the sum of diffusion and subthreshold current so that the waveforms we are getting from the circuits are given the combined value of the both.

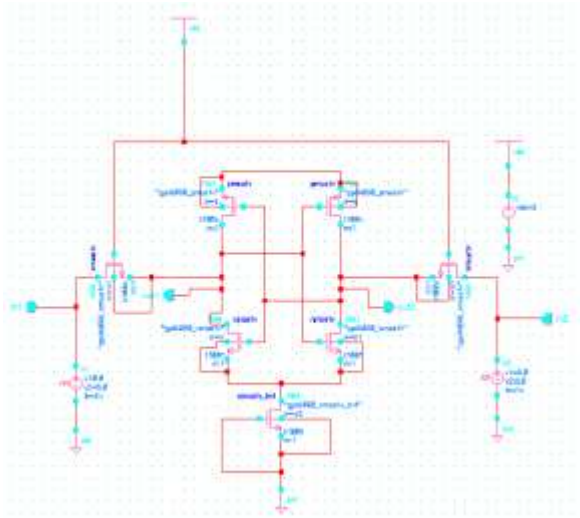


Figure 13 Circuit of the bulk SRAM Cell with sleep transistor

Figure 13 shows the circuit of the bulk 6T SRAM cell and Figure 14 shows the proposed DG-MOSFET based 6T SRAM cell with sleep transistor.

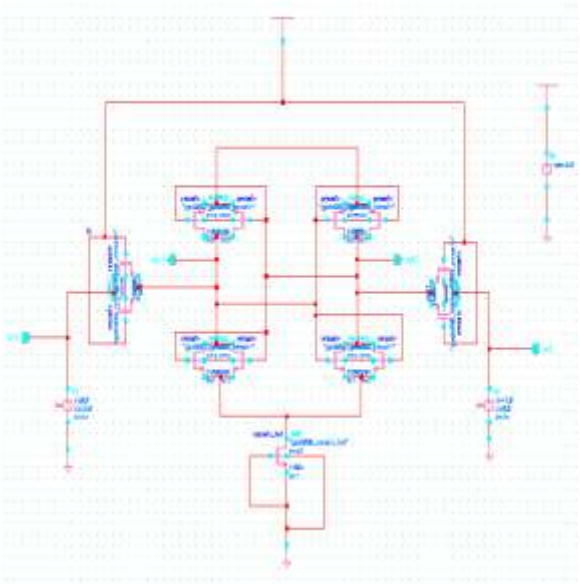


Figure 14 Circuit of the DG-MOSFET Based 6T SRAM Cell with sleep transistor

For getting leakage current of the circuit we are selecting a point of Sleep Transistor. As we know that in the Sleep Transistor the source terminal of the NMOS is connected to the ground so that we can get the value of leakage current from this node of the SRAM circuit.

The comparison table of leakage current for the different values of MOSFET width is given below:

Table 1: Leakage current values with Sleep Transistor at 90nm technology

W/L = x/100	AT THE SOURCE NODE OF	BULK 6T SRAM	DG-MOSFET BASED 6T SRAM
x = 450nm	NMOS	207.45pA	13.759pA
x = 500nm	NMOS	222.77pA	14.759pA
x = 550nm	NMOS	239.40pA	15.766pA
x = 600nm	NMOS	255.43pA	16.983pA
x = 650nm	NMOS	276.32pA	18.012pA

From the Table 1, we can see that by using different feature sizes, we can get different values of the leakage current. As the width of the MOSFET of the bulk 6T SRAM is increased, the leakage current is reduced. The same is done with the DG-MOSFET based SRAM. When we compare the values of leakage current of the bulk 6T SRAM with DG-MOSFET based 6T SRAM, reduction in the leakage current is found which is depicted by the corresponding waveforms.

4. CONCLUSION

With the scaling down of CMOS devices, the progress in technology predicts that Moore's law found difficulty in its existence. As the size of the chip gets reduced, it increases the number of transistors with system's complexity. By combining CMOS with somewhat another platform or add on devices rather than replacing

CMOS technology, will broaden novel application fields in microelectronics which are not recently approachable by CMOS. This integrity is a big benefit of CMOS technology but is also having negative aspects. For instance, memory cell did not provide the capability to merge in an old technology and circuitry. So, we required those technologies which are helpful at low power mode as well as avoid the short channel effect as we move towards the 10nm level. Such architectures which incorporate with technologies are referred to as hybrid architectures.

The proposed designs of SRAM cells and DG-MOSFET based 1bit of 6T SRAM cell is being designed as storage devices. The main disadvantage associated with the CMOS based SRAM cells is the fact that storage circuits based on this technique cannot retain data as well as not works properly in the low power mode, but this problem is also resolved by our proposed circuits that is DG-MOSFET based 6T SRAM cell. Also, with the scaling down of CMOS, power comes into picture as a big issue. Thus, some techniques are used to minimize the rising power dissipation and reduce the other effects. The two approaches or techniques used with the proposed circuits are Sleep Transistor and gated-V_{dd} which are used for diminution of power of the circuits. We aimed to implement DG-MOSFET Based 6T SRAM Cell, analyzed the circuit's performance, and compared it with the conventional SRAM cell for parameter optimization. The simulations were carried out for Representation of DG-MOSFET Based SRAM cells with leakage reduction and threshold. This help to strengthen our proposed work that the DG-MOSFET based memories are better performing as compare to the conventional memories.

The proposed design and implementation of 1-bit of DG-MOSFET based 6T SRAM cell consumes less power, enhances the performance as compared to the existing design of SRAM cell. The device is completely compatible with CMOS. Therefore, researchers and designers are very much interested in MuGFET family especially in double gate devices due to their adjustable low power mode and the reduction of leakage parameters handle carefully without using any techniques. MuGFET's are coming forward as an alternate substitute to CMOS transistors based circuitry with the rising demand for high capacity and lower power consumption in memory devices. Such hybrid architecture combines the flexibility, reliability and functionality of CMOS devices with the less channel length working behaviour of the DG-MOSFET device and provides either the same or increased functionality to the circuit, in terms of providing small size, reduced size and low power. The circuit is simulated under ideal conditions at 27^{o} C temperature using Cadence virtuoso tool at 90 nm technology.

Currently, work is going in several directions. It brings out a set of new possibilities. Its

invention has huge potential in electronics. The future work will be pondered on Leakage current and power for the proposed designs. Other structures like 7T, 8T SRAM cells etc. will also be proposed to calculate various parameters. With the scaling semiconductor devices, insignificant concerns are becoming vital.

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